In the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) ~~Data processing system comprising:~~

- **A** ~~a~~-clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections,

~~one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters,~~ and

one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the **respective** distance**s** between said instruction unit and said plurality of clusters, **the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster** ~~so as to pipeline said control connections to said remote cluster~~.

2. (Currently Amended) **The processor**~~Data processing system~~ according to claim 1, wherein

said clusters are connected to each other via a point-to-point connection.

3. (Currently Amended) **The processor** ~~Data processing system~~ according to claim 1, wherein

said clusters are connected to each other via a bus connection.

4. (Currently Amended) **The processor** ~~Data processing system~~ according to claim 3, wherein

said control connections are implemented as a bus.

5. (Currently Amended) A clustered Instruction Level Parallelism processor, comprising:

- a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections ~~each control connection having a pipeline register~~,

~~one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters,~~ and

one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the **respective** distance**s** between said instruction unit and said plurality of clusters, **the number of additional pipeline registers in a control connection being proportional to the respective distance, to enable a high clock frequency that is not limited by the distance between the instruction unit and the most remote cluster** ~~so as to pipeline said control connections to said remote cluster~~.

6. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a point-to-point connection.

7. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a bus connection.

8. (Previously Presented) The clustered Instruction Level Parallelism processor as claimed in claim 7, wherein said control connections are implemented as a bus.